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Solid-State Circuits, IEEE Journal of, Volume: 29, Issue: 8, Aug. 1994 Pages:972 - 977

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## 2 A high-throughput 5 Gbps timing and jitter test module featuring localized processing

Hafed, M.M.; Chan, A.H.; Duerden, G.; Pishdad, B.; Tam, C.; Laberge, S.; Roberts, G.W.;

Test Conference, 2004. Proceedings. International, 26-28 Oct. 2004 Pages:728 - 737

[Abstract] [PDF Full-Text (1008 KB)] **IEEE CNF** 

# 3 A 16ps-resolution Random Equivalent Sampling circuit for TDR util a Vernier time delay generation

Donghwan Lee; Jinho Sung; Jaehong Park;

Nuclear Science Symposium Conference Record, 2003 IEEE, Volume: 2 25 Oct. 2003

Pages:1219 - 1223 Vol.2

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